FOR IMMEDIATE RELEASE

SiSys AI, Inc, Launches SwitchNoC™, a High-Bandwidth, Low-Latency, Network-on-Chip Switch Fabric IP Designed to Support Next-Generation, Data Center Interconnect Standards.

Los Gatos based company introduces SwitchNoC™ products designed for performance, area and power optimizations, purpose-built to enable the rapid design and deployment of high-performance switch ASICs, powering the future of AI and Cloud.

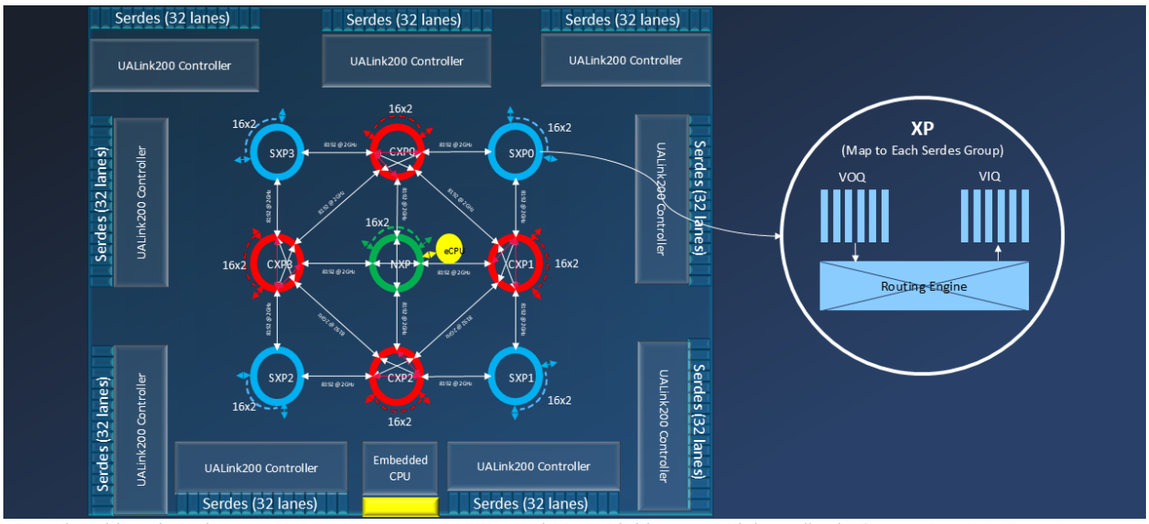
By: SiSys AI, Inc.

LOS GATOS, Calif. – October 1, 2025 – SiSysAI, Inc., a silicon and systems infrastructure company for AI applications, today announced the release of its new SwitchNoC™ fabric IP created to redefine the price/performance ratio for high lane count switch ASICs supporting the latest generation of data interconnect standards. The IP is a critical building block to expediently and efficiently implement switch ASICs needed for scale-out AI system architectures in the box, in the rack, and across the data center.

The 3x3 fabric topology delivers a highly configurable, high-speed, low-latency interconnect architecture designed to optimize data throughput, scalability, and power efficiency for next-generation networking and AI infrastructure. By integrating this compact yet powerful interconnect fabric, chip designers can accelerate time-to-market while ensuring the flexibility required for evolving application demands.

Key Competitive Advantages:

- **Datapath Protocol Support: Seamlessly integrates with leading communication protocols—including UALink, PCIe, CXL, Ethernet, and more—ensuring broad interoperability across AI, HPC, and data center workloads.**
- **Modified 2D Torus Topology: High-efficiency topology delivers non-blocking switching with reduced wire lengths and ultra-low latency. Supports up to 14.4 TBps port switching capacity and industry best latency of 10 to 30ns—ideal for high-throughput chiplet and switch-based architectures.**
- **High-Lane Count Connectivity: SwitchNoC-16 and SwitchNoC-32 provide 144 and 288 lanes of connectivity, respectively.**
- **Integrated VOQs and VIQs: Enhances throughput and fairness with per-port virtual output/input queues.**
- **Multicast/Broadcast Support: Built-in support minimizes redundant traffic, optimizing bandwidth for AI synchronization**
- **Virtual Channels: Improves traffic segregation and QoS enforcement, enabling fine-grained control over priority flows, congestion domains, and arbitration groups.**
- **Physically Cognizant Structure: Placement-aware design significantly improves wire efficiency and routing convergence compared to traditional crossbar architectures. Order-of-magnitude improvement in layout efficiency.**
- **Embedded Management Fabric: Integrates a lightweight embedded management NoC overlaid on the switch fabric to enable intelligent system control, configuration, and diagnostics, supporting comprehensive QoS management for policy enforcement. A built-in mailbox communication mechanism ensures reliable, low-latency message exchange between firmware, software, and hardware agents. Additionally, a unified switch configuration interface provides streamlined access to control registers and runtime parameters, enabling centralized or distributed intelligent switch management.**
- **Power Efficiency: Advanced arbitration and routing algorithms to minimize power per bit transferred.**
- **Design Flexibility: Broad configurability for custom ASIC requirements across networking, AI, storage, and HPC domains.**



"Networking silicon is facing unprecedented demand for bandwidth, flexibility, and efficiency," said George Apostol, Founder, Chairman, and CEO at SiSysAI, Inc. "Our 3x3 SwitchNoC™ IP empowers semiconductor designers with a robust and efficient building block that simplifies complex interconnect challenges, paving the way for the next wave of high-performance switch ASICs. Having built switch products for several decades, this architecture builds on and improves greatly the limitations of switch solutions leading the industry today."

"Our customers are inventing the next generation of networking infrastructure, where every nanosecond and milliwatt make a critical difference," said Dr. Jiebing Wang, PhD, Founder, CTO, and Chief Architect at SiSysAI, Inc. "With SwitchNoC™, we're enabling ASIC engineers with a proven, high-performance interconnect fabric that delivers performance, scalability, and efficiency. This IP not only reduces design complexity and accelerates time-to-market, but also provides the architectural flexibility needed to meet the surging demands of AI, cloud computing, and hyperscale data centers."

SwitchNoC-16 and SwitchNoc-32 are now available for licensing to semiconductor companies, system OEMs, and design houses looking to accelerate their switch ASIC development. SiSysAI, Inc. also provides design services from architecture to volume production as well as turnkey, custom, ASIC design services.

For more information, visit www.sisysai.com : Contact George Apostol, info@sisysai.com

ABOUT SISYS AI, INC.

SiSys AI, Inc. designs and manufactures cutting-edge supercomputers and systems solutions that deliver unmatched computational power and efficiency. By integrating state-of-the-art hardware and software with advanced technology systems and scalable infrastructures, we enable breakthroughs in AI, scientific research, and big data analytics. Our solutions are tailored for industries that demand precision, speed, and innovation. We empower businesses and researchers to tackle the world's most complex challenges.